

**Integrated chip package structure using silicon substrate and method of
manufacturing the same**

Appl. No.	:	10/755,042	Confirmation No.	8665
Applicant	:	Jin-Yuan Lee, Mou-Shiung Lin, Ching-Cheng Huang		
Filed	:	January 9, 2004		
TC/A.U.	:	2815		
Examiner	:	Jackson JR, Jerome		
Docket No.	:	MEGP0004USA1		
Customer No.	:	27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

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RESPONSE TO FINAL OFFICE ACTION

Sir:

In response to the Final Office Action mailed Dec. 10, 2008, please amend the above-identified application and consider the remarks as follows: